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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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23122	7590	11/03/2005	EXAMINER	
RATNERPRESTIA			TERESINSKI, JOHN	
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VALLEY FORGE, PA 19482-0980			2858	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/775,676

Applicant(s)

KISTER ET AL.

Examiner

John Teresinski

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 and 14-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11 and 12 is/are allowed.
- 6) ☒ Claim(s) 1-10 and 14-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

The indicated allowability of claim 15 is withdrawn in view of the newly discovered reference(s) to Velsher and amendment filed 11 August 2005 with broadened claim scope.

Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 9 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,791,344 to Cook et al. in view of U.S. Patent No. 4,491,797 to Velsher.

Regarding claims 1, 2 and 15-17, Cook et al. disclose a probe group having two probes (Fig. 2, elements 30c and 32c), the two probes independently conductively contacting a single test terminal of the circuit chip (Fig. 2, elements 30c, 32c) for determining a path/contact resistance of a single terminal/pad (column 3 lines 5-10) and compensating for voltage drop in correspondence to the operational signal path resistance wherein the resistance value is used in determining a voltage drop compensation for an operational signal configured to pass through the probe apparatus (column 6 lines 7-12, 27-34). Cook et al. does not disclose averaging/dividing by a number/two of the plurality of probes a number of measured test path resistance values, wherein an average resistance value provided by the means for averaging is

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used in determining a voltage drop compensation for an operational signal configured to pass through the probe apparatus. Velsher et al. disclose a tester including a probe having two probes/contacts (column 3 line 1), determining a path/contact resistance (column 1 lines 5-11) and averaging a number of measured test path resistance values, wherein an average resistance value provided by the means for averaging/ dividing by a number (2) of the plurality of probes is used in determining a voltage drop compensation for an operational signal configured to pass through the probe apparatus (column 3 lines 1-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include averaging a number of measured test path resistance values, wherein an average resistance value provided by the means for averaging is used in determining a voltage drop compensation as taught by Velsher into Cook et al. for the purpose of counterbalancing variables in the test circuit such as contact corrosion (column 3 lines 19-21).

Regarding claim 3, Cook et al. discloses the claimed invention except for a third probe conductor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a third probe conductor and perform additional test path resistance measurements, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Regarding claim 9, Cook et al. disclose probe tips that are rotationally symmetric with a non-planar contact surfaces and contact the single terminal in a self centering fashion (Fig. 2 elements 40).

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Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cook et al. and Velsher as applied to claims 1 and 2 above and further in view of U.S. Patent No. 4,667,149 to Cohen et al..

Regarding claim 4, Cook et al. as modified does not disclose a group of four probes and circuitry capable of recognizing a test path resistance according to a 4-Wire Ohm's Measurement. Cohen et al. disclose an electrical test probe apparatus and method for testing a circuit chip/semiconductor (column 3 lines 15-20) comprising a probe group (Fig. 1 elements 10-13) allowing a test path resistance to be measured with a group of four probes and circuitry capable of recognizing a test path resistance according to a 4-Wire Ohm's measurement (column 3 lines 15-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include four probes as taught by Cohen et al. into Cook et al. as modified for the purpose of providing a more detailed characterization of the test path resistance.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cook et al. and Velsher as applied to claim 1 above and further in view of U.S. Patent No. 6,384,614 to Hager et al..

Regarding claim 5, Cook et al. as modified does not disclose buckling beam probes. Hager et al. disclose a single probe group having two probes (Fig. 2, elements 50,60), the two probes having a common contacting center within a probe target area (column 3 lines 15-16), each of the probes independently and conductively contacting within a guiding boundary (84) a single test terminal of a circuit chip with buckling beam/spring probes (column 3 lines 15-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

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include buckling beam/spring probes as taught by Hager et al. into Cook et al. as modified for the purpose of providing a non-invasive test probe.

Claims 6-8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cook et al. and Velsher as applied to claim 1 above and further in view of U.S. Patent No. 4,423,373 to LeCroy.

Regarding claims 6-8, Cook et al. as modified does not teach a bundled probe group in a single perforation of a sheath, a single perforation that is a long hole, or a single perforation in the shape of a circular hole. LeCroy teaches an electrical test probe with bundled probes in a single perforation (Fig. 3A), a long hole (Fig. 3A) and a circular opening (Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a single perforation for the bundled probes, a long hole perforation or a circular opening perforation as taught by LeCroy into Cook et al. as modified for the purpose of permitting longitudinal movement of the probes (column 7 lines 35-40).

Regarding claim 14, Cook et al. disclose the probes having a conductive core and tips (column 3 lines 42-46). Cook et al. as modified does not disclose an insulation layer. LeCroy discloses an insulation layer (48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an insulation layer as taught by LeCroy into Cook et al. as modified for the purpose of preventing an electrical short circuit.

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Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cook et al. and Velsher as applied to claims 1 and 2 above and further in view of U.S. Patent No. 6,218,848 to Hembree et al..

Regarding claim 10, Cook et al. as modified does not disclose essentially spherical probe tips. Hembree et al. disclose probe contacts with essentially spherical shape (column 7 line 11 & Figure 5A). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include spherical probe tips as taught by Hembree et al. into Cook et al. as modified for the purpose of providing an electrically engaging probe tips that establish a good contact (column 7 lines 10-15).

Allowable Subject Matter

Claims 11 and 12 are allowed.

Response to Arguments

Applicant's arguments with respect to claims 1-12, 14 and 15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Teresinski whose telephone number is (571) 272-2235. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on (571) 272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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JT

October 27, 2005



ANJAN DEB
PRIMARY EXAMINER